WHAT IS CLAIMED IS:

1. A display system, comprising:

a standardized display driver to provide address voltages;

an array of interferometric elements; and

a voltage adjuster to adjust address voltages to provide adjusted row address voltages to the array of interferometric elements.

2. The display system of claim 1, the standardized display driver further comprising a driver for a liquid crystal display.

3. The display system of claim 1, the array of interferometric elements further comprising an array if iMoD™ elements.

4. The display system of claim 1, the voltage adjuster further comprising a resistor divider network to lower the address voltage amplitudes.

5. The display system of claim 1, the voltage adjuster to adjust row address voltages.

6. The display system of claim 1, the voltage adjuster to adjust column address voltages.

7. A method of manufacturing an array of modulator elements and an adjuster circuit, comprising:

depositing a first metal layer on a transparent substrate;

patterning and etching the first metal layer to form electrodes;

depositing an optical stack layer;

depositing a first sacrificial layer upon the optical stack layer;

depositing a second metal layer on the sacrificial layer; and

patterning and forming the second metal layer to form modulator elements;

forming resistors from one metal layer and connecting the resistors with a subsequent metal layer.

8. The method of claim 7, forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors with the second metal layer.

9. The method of claim 7, further comprising:

depositing a second sacrificial layer;

depositing a third metal layer on the second sacrificial layer; and

patterning and etching the third metal layer to form posts and supports.

10. The method of claim 9, forming the resistors further comprising forming the resistors from the first metal layer and connecting the resistors using the third metal layer.

11. The method of claim 9, forming the resistors further comprising forming the resistors from the second metal layer and connecting the resistors using the third metal layer.

12. The method of claim 9, further comprising:

depositing a third sacrificial layer;

depositing a fourth metal layer on the third sacrificial layer;

patterning and etching the fourth metal layer to form a bus layer.

13. The method of claim 9, forming the resistors from one metal layer further comprising forming the resistors from the first metal layer and connecting the resistors using the fourth metal layer.

14. The method of claim 9, forming the resistors from one metal layer further comprising forming the resistors from the second metal layer and connecting the resistors using the fourth metal layer.

15. The method of claim 9, forming the resistors from one metal layer further comprising forming the resistors from the third metal layer and connecting the resistors using the fourth metal layer.

16. A resistor network, comprising:

an incoming address line;

a first resistor connected between the address line and a conductive bus; and

a second resistor connected between the address line and an adjusted address line.

17. The resistor network of claim 16, the address line further comprising a row address line.

18. The resistor network of claim 16, the address line further comprising a column address line.